Endpoint Testing (Midpoint Calculation)

by Jerry Antoine

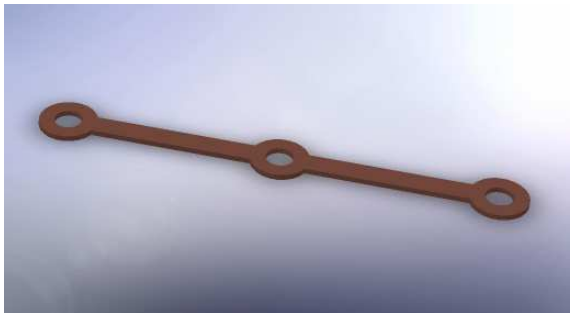
The drive to increase quality while lowering costs has fabricators taking another look at QC. Learning everything you can about the theory of electrical test is the only way you can avoid the pain that would result from finding your QC stamp on a bad board. Knowledge is also the path to reducing cost without adversely impacting test coverage.

Central to the issue of cost is the number of test points. Each unnecessary point adds to complexity and cost without producing any advantage in return. If the point turns out to be in a congested area of the board, it may precipitate a change in class of fixture or test procedure, which in turn would increase cost even more. On the other hand, removing a necessary test point leaves a portion of the board untested and can lead to the aforementioned pain.

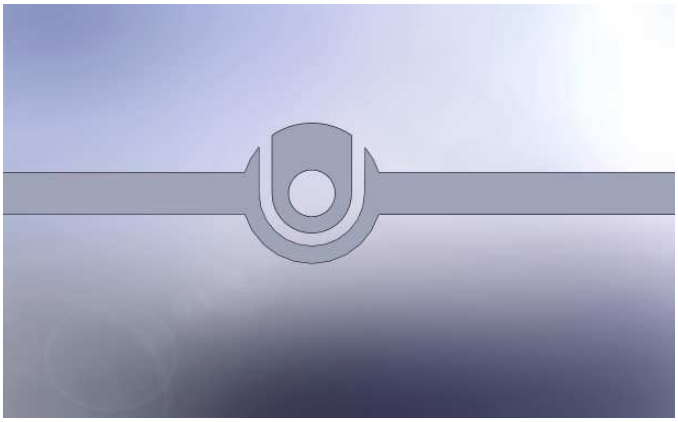
In this article we examine the theory of testing for open circuits, or more specifically "testing for defects in a bare printed-circuit board that might electrically isolate some of a group of points that were intended to be electrically connected to each other by the circuit board".

Three Points in a Line

The most basic example that illustrates the concept of an unnecessary point or "midpoint" is the 'line through three pads'.



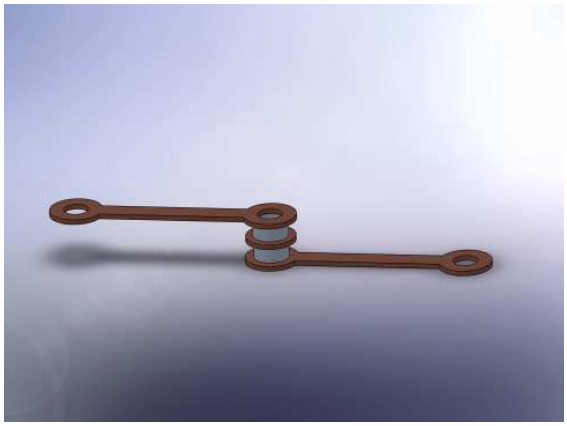
As simple as it is, it makes sense from the standpoint of theory, to examine carefully why it is that we conclude the middle point need not be tested. The middle point need not be contacted because contacting it adds very little information beyond what is already learned by contacting the outer two points. If the trace is "cut anywhere", then that discontinuity will be discovered when a test is applied to the outer two pads. Of course this is not *completely* true.



A devil's advocate might argue that a cut in the shape of a "U" or in the shape of a donut could disconnect the middle pad from the circuit without also disconnecting the end pads from each-other. So by not testing the middle pad, someone is making a statistically valid 'bet' that such a "U" or "O" shaped defect will not occur often enough to offset the cost of testing for it. Generally people are in agreement that the tradeoff is reasonable. The tricky part is defining the types of geometry for which such a bet is, or is not statistically valid.

The Front-to-Back Via

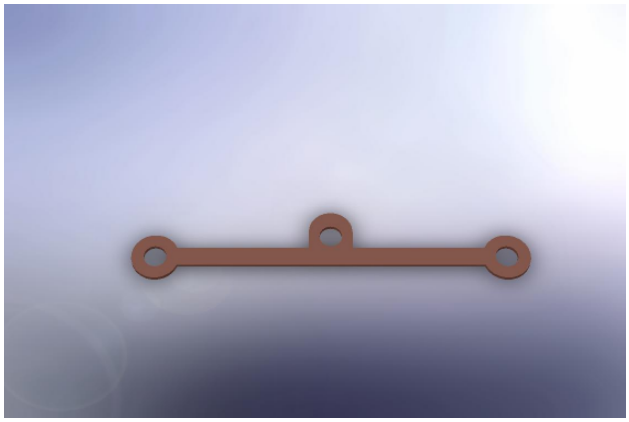
The 'Front-to-Back Via' is another example where there is general agreement as to a test point being unnecessary. In this case, cutting



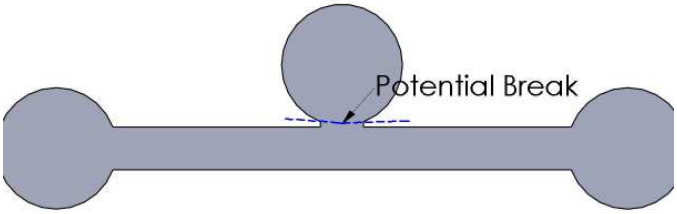
through the traces, or breaking the plating of the hole-barrel will disconnect the endpoints from each other and will therefore be discoverable by testing only the two endpoints. Again, any test probe applied to the via itself will not add significant information.

The 'T' Circuits

The previous examples give us the basis from which we can start to formulate a rule about the necessity of certain test points. The rule is as follows: "A point is required to be tested if and only if *not* testing it would compromise our ability to detect a *reasonable* defect in the circuit". So in order to complete the rule we need to define "reasonable defect".



One reasonable definition would be "An open caused by a scratch or cut in the circuit whose length does not *much* exceed the width of the trace." In other words, we are willing to entertain the likelihood of cuts across a trace, or at a slight angle, but not cuts that run 'lengthwise' along the trace for any great distance.



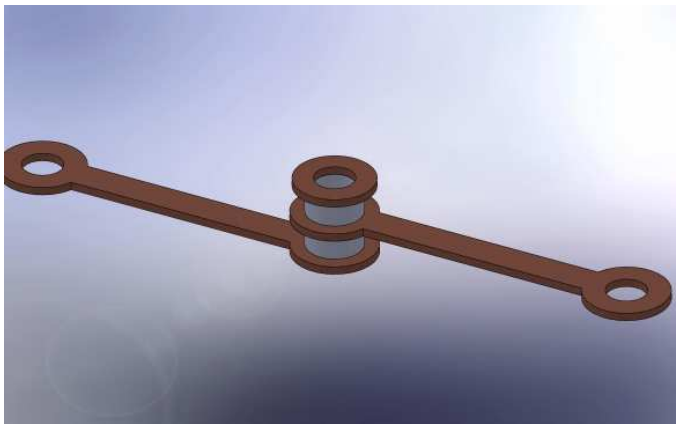
The illustration shows what happens when the pad of the original 'line through three pads' example is slightly modified. In the illustration, the middle point moves in degrees, first to the side of the trace, then eventually into a 'bump' on the side of the trace. Finally it becomes the endpoint of a trace emanating from a "T" branch of the circuit. At some time during this sequence, probing this middle point ceases to be unnecessary and begins to add significant information about a potential 'reasonable' defect. At what point does this happen?

According to our rule, the probe becomes necessary *when the blob of copper that connects the test-point to the main part of the circuit is 'longer than it is wide*'. It is at this point that the likelihood of a break or scratch in the copper becomes statistically significant, and it is at this point that we should put a probe upon the test-point to check for it.

Vias and ICT Points

Internal vias, where a connection is between two inner layers or from an outer to an inner layer raise a different kind of issue. It may be that the part of the hole-barrel that forms part of the circuit has continuity and that the part that does not participate in the circuit is open. If the via were to later be used as an in-circuit test point, then the open would become important. Testing the hole barrels on all vias can often significantly increase the cost of ET.

The problem in this case is not so much deciding whether the defect is probable, but whether it is important.



The designer's direction as to which vias will be used as ICT points allows the test engineer to reduce costs without the risk of mistaking a test point for a via. Often the designer identifies test vias by changing the shape or D-code of the ICT test point.

Unused Pads or Copper

Various copper features on a board are there for cosmetic or for purely mechanical purposes. For example, cosmetic text generally serves no electrical purpose. Plated lands on non-plated mounting holes may also have no electrical significance. That these features have no electrical use does not necessarily mean that they can be ignored. Their accidental connection to a circuit may significantly change the electrical characteristics (impedance) of the circuit. In addition, they may act as a kind of bridge between two circuits, thereby causing a short. When testing with a fixture, the short so-caused would be detected between the two circuit nets. When testing with a flying-probe tester, however, the short might be missed as the circuit nets may not come closer to each-other than the adjacency air-gap parameter used in the netlist generation software.

Circuits with Inaccessible Ends

Occasionally a circuit has an endpoint that is either not testable with the customer's available tester, or completely inaccessible. If the endpoint pads are too small to test with a universal tester, the test may be split into two passes. The first pass can be performed with the universal tester. It may be possible to also perform the second pass on the universal tester by using clever fixturing techniques. More often however, second-pass testing is done on a flying probe machine. The flying probe can use optical alignment to find fine features that may have moved slightly during the board fabrication process.

In the case that the points are truly inaccessible, the circuit should be tested using the 'next-best' point.

Loops

A circuit that has one or more loops presents an interesting challenge. When loops are present, a trace can often be completely cut without affecting the connectivity of the board. The affected net may have lower current-carrying capacity and a change in impedance, but these are not typically measured by bare-board testing equipment. Also, the number of points to test on a loop is often debated. Some argue that heavily connected loops should be tested at one point. Others maintain that two points should be the accepted minimum.

Planes

Planes present challenges similar to those of loops. It is typically difficult to electrically separate a pad imbedded in a plane unless the pad is separated from the main body of the plane by thermal-reliefs or by the barrel of a plated hole.

All-Components Test – Board Intent

One theory suggests that boards are only guaranteed good if they are tested to all points where a component or device will eventually

connect. The main impediment to this type of testing is information. Very often the data given by designers to fabricators has conflicts. The data that is most nearly correct is usually the circuit-board artwork. When component locations do not completely agree with the artwork, it is usually the artwork that is given priority.

The method preferred by the author is to use artwork as the means for *targeting* probes. Only the artwork has the exact geometry of the circuits. In order to eliminate contradictions and confusion with the customer's netlist, a 'net compare' is performed. The net compare lists any discrepancies, and these should be explained or corrected before the board is fabricated.

Test Software

A fabricators greatest weapon against improper testing and customer returns is the ET software that was used to generate the test. If the test software takes several 'tries' to get the net list correct, then it follows that other calculations may be equally temperamental. Incorrect net lists are easily discovered when the tester complains of an open or a short. Missing test points, incorrect midpoint calculations and bad adjacency lists, however, may silently slip by unnoticed. In these cases, the fabricator is unknowingly exposed to the liability that results from shipping boards that are not fully tested. Quite a few CAM systems that claim to produce ET files have these very significant issues.

Conclusion

High-quality fabricators know that ET is not just a 'necessary evil' but instead a way to differentiate themselves from their lower-quality competitors. Accurate selection of test points is critical to combining efficiency with quality. We hope the concepts presented here will help improve your test department and your bottom line.

Jerry Antoine, the author of this article, is president of GCA Technology International, Inc., a company that makes high-end ET software for the printed circuit fabrication market. GCA's software is used by high profile fabricators in a dozen countries throughout the world - many of whom switched to GCA after use of other software cost them dearly in the form of expensive returns and/or lost customers. GCA software is also the system of choice with high-end fixture and test service bureaus.

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